IN THE CLAIMS:

Please cancel claim 2 without prejudice or disclaimer and accept amended claims 1, and 7-9 and new claim 41 as follows:

1. (currently amended) A thin film transistor array panel comprising:

a substrate;

a plurality of first signal lines formed on the substrate, extending in a first direction, and separated from each other by a predetermined interval;

a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions and intermediate portions extending in a second direction and alternately arranged by the predetermined interval, wherein the intermediate portions intersect the first signal lines and extend from the curved portions at an angle with respect to the curved portions, and wherein each of the curved portions of the plurality of second lines comprises a pair of rectilinear portions connected to each other and making an angle of about 90 degrees;

a plurality of pixel electrodes located substantially in areas defined by the first and the second signal lines; and

a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes.

2. (canceled)

3. (original) The thin film transistor array panel of claim 1, further comprising a

plurality of third signal lines formed on the substrate, extending substantially in the first direction, and overlapping the pixel electrodes to form storage capacitors.

4. (original) The thin film transistor array panel of claim 3, wherein the thin film transistors include terminal electrodes connected to the pixel electrodes and overlapping one of the third signal lines with interposing an insulator.

5. (original) The thin film transistor array panel of claim 1, wherein the thin film transistors include terminal electrodes connected to the intermediate portions of the second signal lines.

6. (original) The thin film transistor array panel of claim 1, wherein the first signal lines intersect the intermediate portions of the second signal lines.

7. (currently amended) A thin film transistor array panel comprising:

a substrate;

a gate line formed on the substrate and including a gate electrode;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data line formed on the semiconductor layer at least in part and including a curved portion and an intermediate portion crossing the gate line substantially at a right angle, at least one of the curved portions and the intermediate portions having a source electrode, wherein the intermediate portion extends from the curved portion

at an angle with respect to the curved portion;

a drain electrode formed on the semiconductor layer at least in part and separated from the data line;

a first passivation layer formed on the data line and the drain electrode;

[[and]]

a pixel electrode formed on the first passivation layer, connected to the drain electrode, and having an edge extending substantially parallel to the curved portion of the data line; and

a storage electrode line formed on the substrate, extending substantially parallel to the gate line, and including a storage electrode having an increased width with respect to a width of the storage electrode line.

8. (currently amended) The thin film transistor array panel of claim 7, wherein the curved portion of the data line comprises a pair of portions making a clockwise angle of about 45 degrees and a counterclockwise angle of about 45 degrees with the gate line, respectively.

9. (currently amended) The thin film transistor array panel of claim 7, ~~further comprising a storage electrode line formed on the substrate, extending substantially parallel to the gate lines, and including a storage electrode having an increased width with respect to a width of the storage electrode line,~~ wherein the drain electrode has an expansion connected to the pixel electrode and overlapping the storage electrode.

10. (original) The thin film transistor array panel of claim 7, wherein the first passivation layer comprises organic insulating material.

11. (original) The thin film transistor array panel of claim 7, wherein the first passivation layer is made of photosensitive material.

12. (original) The thin film transistor array panel of claim 7, wherein the first passivation layer comprises inorganic insulating material.

13. (original) The thin film transistor array panel of claim 12, further comprising a color filter formed on the first passivation layer.

14. (original) The thin film transistor array panel of claim 13, wherein the color filter extends substantially parallel to the data line.

15. (original) The thin film transistor array panel of claim 13, wherein the color filter has an opening on the drain electrode, the first passivation layer has a contact hole exposing at least a portion of the drain electrode, and the pixel electrode is connected to the drain electrode through the opening and the contact hole.

16. (original) The thin film transistor array panel of claim 15, wherein the opening exposes a top surface of the first passivation layer.

17. (original) The thin film transistor array panel of claim 13, further comprising a contact assistant formed on a portion of the gate line or a portion of the data line and made of the same material as the pixel electrode.

18. (original) The thin film transistor array panel of claim 17, wherein the color filter includes a portion formed under the contact assistant.

19. (original) The thin film transistor array panel of claim 13, further comprising a second passivation layer formed on the color filter and made of a photosensitive organic material.

20. (original) The thin film transistor array panel of claim 19, wherein the first and the second passivation layers have a contact hole that exposes at least a portion of the drain electrode and has a sidewall making an angle of about 30 degrees to about 85 degrees with a surface of the substrate, and the pixel electrode is connected to the drain electrode through the contact hole.

21. (original) The thin film transistor array panel of claim 19, wherein the first and the second passivation layers have a contact hole that exposes at least a portion of the drain electrode and has a stepped sidewall, and the pixel electrode is connected to the drain electrode through the contact hole.

22. (original) The thin film transistor array panel of claim 13, wherein entire bottom surfaces of the data line and the drain electrode are disposed substantially on the semiconductor layer, the data line and the drain electrode have substantially the same planar shape as the semiconductor layer, and the semiconductor layer includes a portion that is not covered with the data line and the drain electrode and disposed between the source electrode and the drain electrode.

23. (original) The thin film transistor array panel of claim 7, wherein a length of the curved portion of the data line is about one to nine times a length of the intermediate portion of the data line.

24. (original) The thin film transistor array panel of claim 7, further comprising a pair of color filters formed on the first passivation layer and partly overlapping each other to form a hill.

25. (original) The thin film transistor array panel of claim 24, further comprising a second passivation layer formed on the color filters and forming a projection on the hill of the color filters.

26. (withdrawn) A liquid crystal display comprising:

a first substrate;

a plurality of first signal lines formed on the substrate;

a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions;

a plurality of pixel electrodes located substantially in areas defined by the first and the second signal lines;

a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes;

a second substrate facing the second substrate;

a common electrode formed on the second substrate;

a region partitioning member formed on at least one of the first and the second substrates; and

a liquid crystal layer disposed between the first substrate and the second substrate and partitioned into a plurality of tilt regions by the region partitioning member, each tilt region including a pair of major edges parallel to the curved portions of the second signal lines.

27. (withdrawn) The liquid crystal display of claim 26, wherein the liquid crystal layer has negative dielectric anisotropy and is subject to vertically alignment.

28. (withdrawn) The liquid crystal display of claim 26, wherein the region partitioning member comprises a plurality of cutouts formed in the common electrode.

29. (withdrawn) The liquid crystal display of claim 29, wherein the cutouts have width ranging about 9 microns to about 12 microns.

30. (withdrawn) The liquid crystal display of claim 26, wherein a distance between

the major edges of each region is in a range between about 10 microns and about 30 microns.

31. (withdrawn) The liquid crystal display of claim 26, wherein the tilt regions are classified into four domains based on tilt directions of liquid crystal molecules included therein upon application of an electric field.

32. (withdrawn) The liquid crystal display of claim 26, wherein the number of the tilt regions in a pixel region defined by the first signal lines and the second signal lines is four if a planar area of the pixel region is smaller than about 100x300 square microns, and the number of the tilt regions in a pixel region defined by the first signal lines and the second signal lines is four or eight if a planar area of the pixel region is equal to or larger than about 100x300 square microns.

33. (withdrawn) The liquid crystal display of claim 26, wherein a pair of crossed polarizers are provided on outer surfaces of the first and the second substrates, respectively, and the first and the second polarizers are aligned so that one of the transmissive axes of the polarizers be parallel to the first signal lines.

34. (withdrawn) The liquid crystal display of claim 26, wherein the region partitioning member comprises a protrusion formed on the common electrode and having a width ranging about 5 microns to about 10 microns.

35. (withdrawn) A liquid crystal display comprising:

a first substrate;

a plurality of first signal lines formed on the substrate;

a plurality of second lines formed on the substrate, intersecting the first signal lines, and including a plurality of curved portions;

a plurality of pixel electrodes located substantially in areas defined by the first and the second signal lines;

a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes;

a second substrate facing the second substrate;

a common electrode formed on the second substrate;

a region partitioning member formed on at least one of the first and the second substrates; and

a liquid crystal layer disposed between the first substrate and the second substrate and partitioned into a plurality of tilt regions by the region partitioning member,

wherein liquid crystal molecules included in each tilt region tend to tilt in a direction parallel to an electric field generated between adjacent pixel electrodes.

36. (withdrawn) The liquid crystal display of claim 35, wherein a pair of crossed polarizers are provided on outer surfaces of the first and the second substrates, respectively, and the first and the second polarizers are aligned so that one of the transmissive axes of the polarizers be parallel to the first signal lines.

37. (previously presented) The thin film transistor array panel of claim 1, wherein the angle with respect to the curved portions is about 135 degrees.

38. (previously presented) The thin film transistor array panel of claim 7, wherein the angle with respect to the curved portion is about 135 degrees.

39. (previously presented) The thin film transistor array panel of claim 1, wherein the intermediate portions connect curved portions at each end of the intermediate portions.

40. (previously presented) The thin film transistor array panel of claim 7, wherein the intermediate portion connects curved portions at each end of the intermediate portion.

41. (new) The thin film transistor array panel of claim 9, wherein edges of the expansion are substantially parallel to edges of the storage electrode.